Remarks

This communication is responsive to the Non-Final Office Action of **February 24, 2009.** Reexamination and reconsideration of the remaining claims is respectfully requested.

Status of Claims

Claims 1, 5-10, 13-18, and 20-24 are pending for examination.

Claims 2, 3, 4, 11, 12, and 19 were previously canceled.

Claims 1, 5-10, 13-18, and 20-24 are amended herein.

Claims 1, 10, and 18 are in independent form.

Summary of The Office Action

The claims were objected to because of acronyms that were not spelled out, and because of other typographic errors (e.g., "from card" instead of "front card"). The claims have been amended as suggested by the Examiner.

Claims 1, 5-10, 13-18 and 20-24 were rejected under 35 USC §103(a) as purportedly being unpatentable over applicant's admitted prior art (AAPA) in view of Bachrach, Yuval (US 6,694,394)(Bachrach).

Response

The Claims Patentably Distinguish Over the References of Record

35 U.S.C. §103

To establish a prima facie case of 35 U.S.C. §103 obviousness, basic criteria must be met. The prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2143.(A) Section 2131 of the MPEP recites how "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). This same standard applies to 103 rejections as evidenced by Section 2143(A) of the MPEP, which reads: "The rationale to support a conclusion that the claim would have been obvious is that **all the claimed elements** were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions".

Additionally, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). This requirement is intended to prevent unacceptable "hindsight reconstruction" where Applicant's invention is recreated from references using the Application as a blueprint.

Here, the criteria for establishing a prima facie case of obviousness are not satisfied since the combination of references does not teach or suggest all the claim limitations. None of the references, alone and/or in combination, teach disabling a connection on a router's IDSEL pin when an FE PHY (fast Ethernet physical layer

device) is not present on a back card in the router. Thus, none of the claims are obvious for at least this reason.

Independent Claims 1, 10, 18

Claim 1 recites a method for detecting the absence of a PHY layer device on a back card. Independent claims 10 and 18 recite similar elements and limitations in different claim formats (e.g., apparatus, means plus function).

The method is performed in a router having a front card. The front card is a PCI-compliant device that is an FE MAC. The back card to be detected is an FE PHY. The method includes receiving a sensing signal. The sensing signal is received by a switching input of a tri-state buffer on the front card. If the signal is low, then an IDSEL signal is coupled in a first way. If the signal is not low, then the IDSEL signal is decoupled in a second way. The sensing and coupling are clearly illustrated in the application as originally filed.

As stated on pages 13 and 14 of the application as originally filed, "when a FE PHY is present, the switch 116 is opened, the IDSEL connection 106 is coupled to the FE MAC 110, and the back card will be coupled to the front card via the bus per normal PCI procedures." Page 13, lines 8-10. "When the switch 116 is closed, the IDSEL connection 106 is decoupled from the FE MAC 110." Page 14, lines 1-2. Thus, particular sensing and switching are claimed and described.

The Office Action asserts that the "Applicant's Admitted Prior Art" (AAPA) teaches "receiving by the input of circuit 105, provided on a PCI-compliant front card comprising an FE MAC in a router." This is incorrect and irrelevant. The claim recites "receiving, **by a switching input** of a tri-state buffer". The background section, and figure 2, show a front card with an FE MAC, but **no switching input**.

The Office Action asserts that the AAPA teaches "receiving ... a sensing signal ... where the ... is serially disposed on an IDSEL line." This is also incorrect.

To the extent that a "sensing signal" is show in figures 1 or 2, and described in the background section, the "signal" comes from an ID PROM 104. The line from ID PROM 104 is not connected to the IDSel line.

The Office Action asserts that "the IDSEL input is driven high in combination of Command/byte enable signals 'C/BE during a config cycle for making active or present of the device, and vice versa." This sentence is unreadable, and appears to be irrelevant. The claim recites "if the sensing signal is logical low" taking one action, and "if the sensing signal is not low" taking a different action. The Office Action talks about driving IDSEL based on command/byte enable, not based on the output of a tri-state buffer.

The Office Action agrees that the background section does not describe the "tri-state buffer". The Office Action then asserts that Bachrach "discloses the method and interface circuits within the MAC and PHY allow for MAC to detect if a PHY is present or connected." Once again this statement is both difficult to read and likely irrelevant. Recall that the Office Action is relying on Bachrach to teach the missing tri-state buffer receiving a sensing signal on a switching input of the tri-state buffer, where the sensing signal comes from the back card and facilitates identifying whether the back card has an FE PHY. Bachrach does not show this.

The Office Action asserts that figures 9 and 11 show the circuitry, (e.g., the tri-state buffer). There is clearly no tri-state buffer in figure 9, there are just some lines between a MAC and a PHY. Similarly, there is clearly no tri-state buffer in figure 11. Once again there are just some lines between a MAC and two PHYs. Applicant respectfully requests that the Examiner provide a numerical citation to which element on either figure 9 or figure 11 is the missing tri-state buffer.

The Office Action asserts that the abstract teaches the circuitry (e.g., tri-state buffer).

The following table provides phrase by phrase analysis of the abstract and reveals that the missing tri-state buffer is not taught.

Phrase	Teaches Missing Tri-State Buffer?
A word-based interface between a MAC and a PHY,	No
Allowing for variable pin counts,	No
Variable PHY and MAC data speeds,	No
And variable numbers of connected PHYs.	No
The word-based interface allows for the PHY to provide PHY-to-MAC words to the MAC,	No
And for the MAC to provided MAC-to-PHY words to the PHY,	No
Where the PHY-to-MAC words are synchronized with the MAC-to-PHY words.	No
Data and commands are provided in fields of the words,	No
And may be time multiplexed over the interface.	No
Circuits within the MAC and PHY allow for the MAC to detect if a PHY is present,	No
The number of active pins	No
And the number of PHYs connected.	No
The reset and synchronization signals are integrated into a single reset/sync signal.	No
Identification data is exchanged between the MAC and PHY so that the proper device driver for the PHY may be loaded independently of the BIOS.	No.

While the abstract says there are "circuits within the MAC and PHY", it does not say what those circuits are. It is likely that to the extent there are any circuits in the MAC and PHY tasked with determining whether the FE PHY is present, those circuits are simply the prior art circuits described in the background section of the current application.

Figure 10 illustrates an input buffer 1012. Input buffer 1012 does not appear to be a tri-state buffer associated with determining whether a back card includes an FE PHY. Instead, input buffer 1012 is used to selectively transmit data received on an input pin. Col. 6, lines 36-43 describe the usage of input buffer 1012. These lines recite "If the output of input buffer 1012 is sensed HIGH, then FSM 1010 determines the RxDi 1002 is not connected, in which case the output of input buffer 1012 is not strobed. If, however, the output of input buffer 1012 is sensed LOW, then FSM 1010 determines that RxDi 1002 is connected to PHY 126, in which case the output of input buffer 1012 is strobed every clock cycle to provide communication between MAC 124 and PHY 126." This passage, and indeed the entire reference, is completely silent about the claimed receiving of a sensing signal that is used to control the coupling/decoupling of IDSEL.

Bachrach does not even mention an IDSEL line. It is improper to combine a reference that does not have a tri-state buffer that does not receive a sensing input that does nothing to control coupling an IDSEL line with the applicant's background section where an IDSEL line appears. Even if Bachrach was combined with the AAPA, the combination would still not teach the elements of the independent claims. Specifically, even if the input buffer 1012 of Bachrach was added to front card 100, the input to the input buffer 1012 could not control a switch that controls the IDSEL line because it is the finite state machine 1010 that controls any "switching" associated with input buffer 1012.

The input buffer 1012 is connected to a finite state machine 1010. The office action asserts that there is a pull-up circuit 1006 on the MAC and a pull down circuit

1008 on the PHY. While applicant does not agree with the characterization of these elements, applicant has, never the less, amended independent claims to recite that both the pull up and pull down components associated with the tri-state buffer are located on the front card. Thus, for at least this reason, Bachrach does not make the amended claims obvious. Therefore, none of the dependent claims are obvious either.

For at least these reasons, none of the claims are obvious over Bachrach and the AAPA. Therefore Applicant respectfully requests allowance of the remaining claims.

CONCLUSION

For the reasons set forth above, the claims are now in condition for allowance. An early allowance of the claims is earnestly solicited.

Respectfully submitted,

Date: May 4, 2009

John T. Kalnay, Registration No. 46,816
KRAGULJAC & KALNAY, LLC
Customer No. 76863
4700 Rockside Road
Summit One, Suite 510
Independence, OH 44131
Telephone: 216.308.3245
Facsimile: 216.503.5401